LOW TCR HIGH RESISTANCE RESISTOR

BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced rapid growth in recent years. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. However, these advances have increased the complexity of processing and manufacturing ICs and, for these advances to be realized, similar developments in IC processing and manufacturing are needed. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component that can be created using a fabrication process) has decreased.

Semiconductor resistors may be formed on ICs. It is desirable for such resistors to have a low temperature coefficient of resistance (TCR) while also having a high resistance. Traditionally, methods for reducing TCR while maintaining high resistance involved extra film deposition (either polysilicon or SiCR), extra masks, and/or higher costs. In addition, these processes were complicated and sometimes resulted in residue or damage to the device.

Therefore, while existing methods of fabricating semiconductor resistors have been generally adequate for their intended purposes, they have not been entirely satisfactory in every aspect.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a flowchart illustrating a method for fabricating a semiconductor device according to various aspects of the present disclosure.

FIGS. **2-8** are diagrammatic fragmentary cross-sectional side views of a portion of a semiconductor device according to various aspects of the present disclosure.

FIG. **9** is a perspective view of a portion of a semiconductor device according to various aspects of the present disclosure.

FIG. **10**A is a two-axis line graph plotting the temperature coefficient of resistance and sheet resistance for different thicknesses of polysilicon.

FIG. **10**B is a table providing implantation parameters for the different data points in FIG. **10**A.

DETAILED DESCRIPTION

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of various embodiments. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Illustrated in FIG. **1** is a flowchart of a method **20** for fabricating a semiconductor device according to various aspects of the present disclosure. Referring to FIG. **1**, the method **20** begins with block **21** in which a substrate including a top surface is provided. The method **20** continues with block **22** in which a gate is formed over the top surface of the substrate. The formed gate has a first height measured from the top surface of the substrate. The method **20** continues with block **23** in which the gate is etched to reduce it to a second height. This second height is substantially less than the first height. The processes performed by blocks **21**, **22** and **23** result in the formation of a gate that is substantially thinner than other gates formed on the substrate that were not subjected to the etching of block **23**.

FIGS. **2-8** are diagrammatic fragmentary cross-sectional side views of a portion of a semiconductor device according to various aspects of the present disclosure. Referring FIG. **2**, a semiconductor device **30** including a substrate **40** is shown. An active region **50** is formed in the substrate **40** using one or more ion implantation processes known in the art. In certain embodiments, the active region **50** is formed when the substrate **40** is doped with a P-type dopant such as boron. In other embodiments, an N-type dopant such as arsenic or phosphorous is used. In certain embodiments, doped wells are also formed in the active region **50** using one or more implantation processes. For the sake of simplicity and clarity, these doped wells are not specifically illustrated herein. Isolation structures such as shallow trench isolation (STI) device **60** are also formed in the substrate **40**. The STI device **60** includes a dielectric material, which may be silicon oxide or silicon nitride. The STI device **60** is formed by etching a trench in the substrate **40** and thereafter filling the trench with the dielectric material.

A gate **70** is formed over the substrate **40**. The gate **70** includes a gate dielectric layer **80** and a gate electrode layer **90** that is formed over the gate dielectric layer. The gate dielectric layer **80** includes an oxide material. The gate electrode layer **90** includes a polysilicon material. Gate spacers **100** are also formed on the side walls of the gate **70**. In certain embodiments, the gate **70** functions as a resistor.

A gate **110** is also formed over the substrate. The gate **110** includes a gate dielectric layer **80** and a gate electrode layer **90** that is formed over the gate dielectric layer. In certain embodiments, the gate dielectric layer **80** includes an oxide material. In other embodiments, the gate dielectric layer **80** includes a high-k dielectric material. The high-k material can be defined as a dielectric material having its dielectric constant greater than about 3.9, that of a thermal silicon oxide. For example, the high-k dielectric material may include hafnium oxide (HfO2), which has a dielectric constant that is in a range from approximately 18 to approximately 40. Alternatively, the high-k material may include one of ZrO2, Y2O3, La2O5, Gd2O5, TiO2, Ta2O5, HfErO, HfLaO, HfYO, HfGdO, HfAlO, HfZrO, HfTiO, HfTaO, SrTiO, or combinations thereof. In certain embodiments, the gate electrode layer **90** includes a polysilicon material. In other embodiments, the gate electrode layer **90** includes a metal material such as tungsten, aluminum, copper, or combinations thereof. Gate spacers **100** are formed on the side walls of the gate **110**.

The gate **70** has a height **150** measured from the top surface of the substrate **40**. The gate **110** has a height **160** measured from the top surface of the substrate **40**. In the depicted